IN THE SPECIFICATION:

Please amend paragraph 14 of the specification as shown below.

Turning now to FIG. 1, a block diagram of one embodiment of a computer system 10 is shown. Computer system 10 includes a plurality of processors 20-20n connected to a memory subsystem 50 via a system bus 25. Memory subsystem 50 includes a memory controller 30 coupled to a system memory 40 via a memory bus 35 and a serial bus 37. It is noted that, although two processors and one memory subsystem are shown in FIG. 1, embodiments of computer system 10 employing any number of processors and memory subsystems are contemplated. In addition, elements referred to herein with a particular reference number followed by a letter may be collectively referred to by the reference number alone. For example, processor 20A-n may be collectively referred to as processor 20.

Please amend paragraph 24 of the specification as shown below.

In the illustrated embodiment, memory module 100A is configured to receive address, control and data signals as well as a serial data from a memory controller such as memory controller 30 of FIG. 1, for example. In the illustrated embodiment, memory module 100A is coupled to address signals ~~A0-A13~~ AD0-AD13 and control signals CAS0/, CAS1/, RAS0/, RAS1/, CKE0, CKE1, WE0, WE1, CS0/, CS1/, CLK+, and CLK-. In addition, memory module 100A is coupled to 144 data signals. In the illustrated embodiment, the data signals are designated as DQ0-DQ143. However, as described above, each memory module may include 144 data signals and they may be designated DQ144-287, or DQ288-431, etc... Memory module 100A is also coupled to a serial interface (e.g. serial bus 37) such as an Inter-IC (I2C®) bus, developed by Philips Semiconductors, Inc., for example, for connection between SPD 275 and the memory controller. It is noted that signal names followed by a '/' are indicative of active low signals.

Please amend paragraph 34 of the specification as shown below.

In the illustrated embodiment, memory module 100B is configured to receive address, control and data signals as well as a serial data from a memory controller such as memory controller 30 of FIG. 1, for example. In the illustrated embodiment, memory module 100B is coupled to address signals ~~A0-A13~~ AD0-AD13 and control signals CAS0/, CAS1/, RAS0/, RAS1/, CKE0, CKE1, WE0, WE1, CS0/, CS1/, CLK+, and CLK-. In addition, memory module 100B is coupled to 144 data signals. In the illustrated embodiment, the data signals are designated as DQ0-DQ143. However, as described above, each memory module may include 144 data signals and they may be designated DQ144-287, or DQ288-431, etc. Memory module 100B is also coupled to a serial interface (e.g. serial bus 37) such as an Inter-IC (I2C®) bus, developed by Philips Semiconductors, Inc., for example, for connection between SPD 375 and the memory controller.